AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 13, line 20 – page 14, line 10 with the following amended paragraph.

Figure 4 shows an example of a preferred embodiment of the present invention, wherein the power grid 400 lines are discontinuous in the vicinity of the spiral inductor 402 to minimize mutual inductance that would otherwise occur. (It should be noted that in Figure 4, the grid 400 represents the power grid, not the clock distribution grid.) The power grid 400 may represent, for example, alternating power and ground lines, a single power level (e.g., GND or V_{dd}) or, a combined power grid with each line representative of multiple of different power lines, provided that power lines within the vicinity of the inductor 402 are similarly discontinuous. So preferably, the power grid discontinuities form a fingered gap 404 pattern in both vertical and horizontal power grid lines in the immediate vicinity of the spiral inductor 402 to minimize local power grid wire loops without interrupting local power distribution. So, even though grid wires in this area are discontinuous, the grid 400 remains sufficiently intact to deliver power locally, including to devices/circuits under the inductor. However, the wire gaps prevent current-loops that could otherwise occur in a typical continuous power grid [[with]]. Thus, the performance losses to otherwise normally induced currents in the power grid are avoided. Since the power grid 400 still covers all parts of the chip, even the area below the inductors 402 can be utilized by other circuits or for decoupling capacitors. Therefore, the area occupied by the inductors 402 does not significantly impact/increase chip area as it might otherwise have.